

Sub-20nm Gate definition for MESFET/MOSFET IC applications

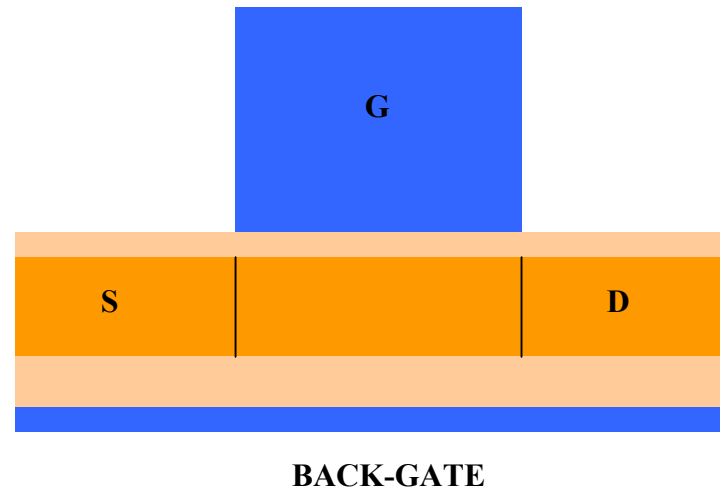
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EE290B Project Presentation
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Outline

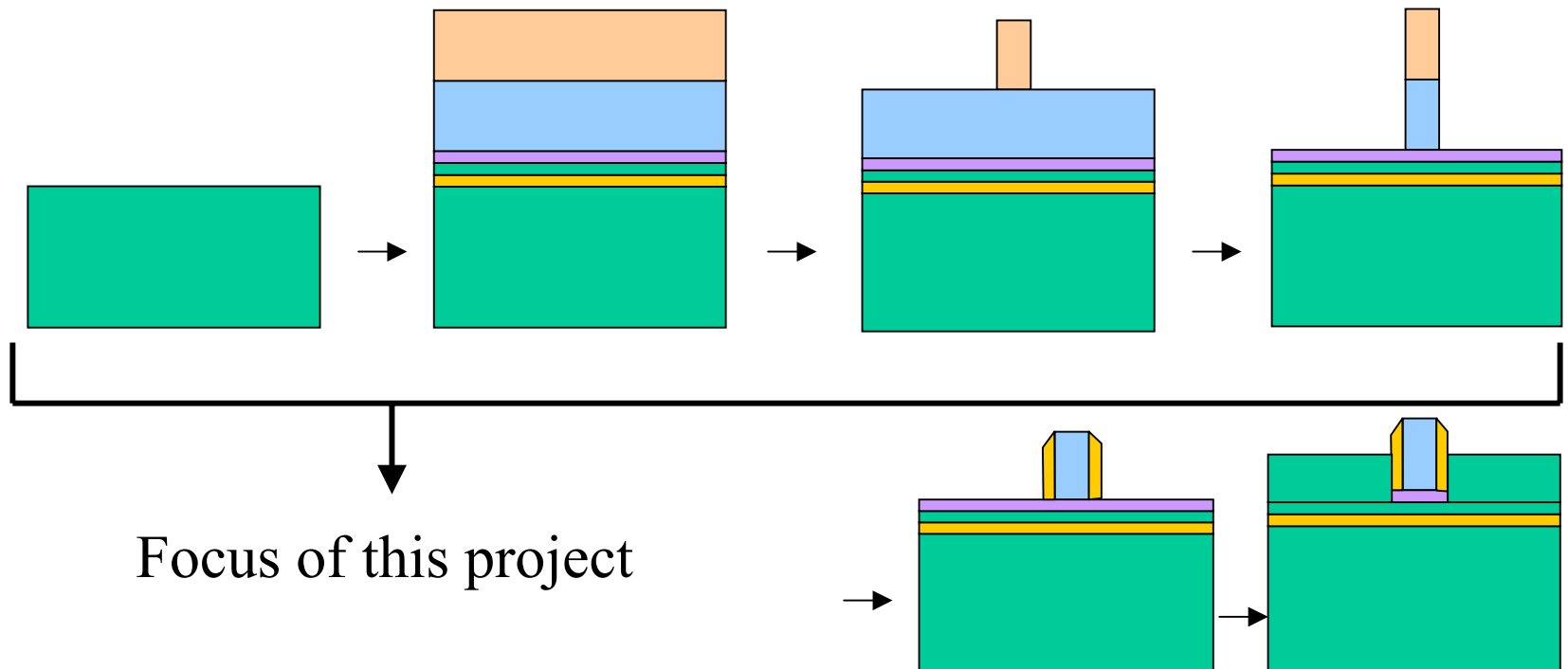
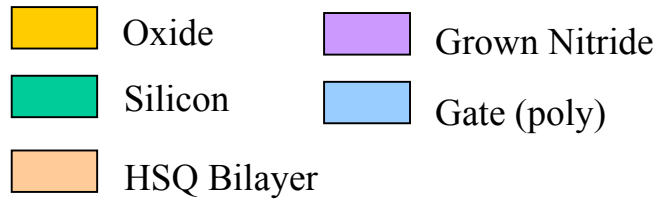
- Motivation for the study
- Process details
- Experimental results
- Possible causes behind observed failures
- Conclusions

Motivation: Going beyond the end of the Roadmap

- ITRS roadmap shows 9nm technology node as the end
- MESFETs are possible solutions beyond 9nm
 - Simple to fabricate
 - Better performance
 - Low power consumption

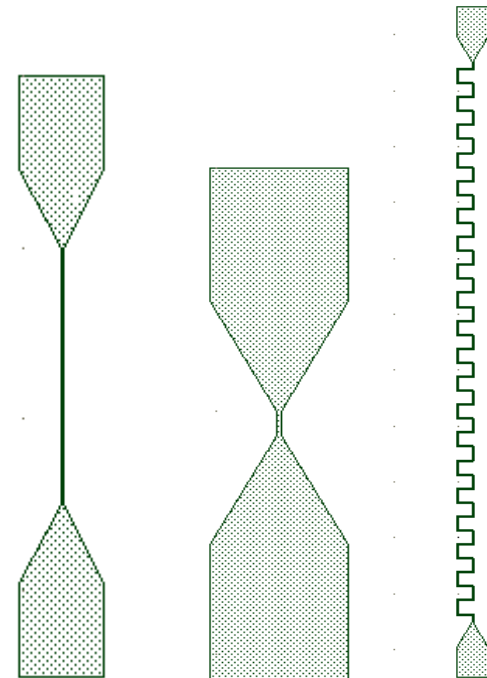


MESFET process flow



Process details 1: Layout

- Layout done using Cadence
- Channel lengths from 12nm to 90nm
- Channel widths from 100nm to 15 μ m
- Wiggles introduced to improve mechanical stability of the gate: wider gates feasible.



Process details 2: exposure and ashing conditions

- Resist used : HSQ bilayer composed of 15% HSQ on 1.8% AZPN
- Exposure : Field size : $131\mu\text{m} \times 131\mu\text{m}$
 - Exposure 1: Dose range $400 \mu\text{C}/\text{cm}^2$ - $1600 \mu\text{C}/\text{cm}^2$
 - Exposure 2: Dose range $1100 \mu\text{C}/\text{cm}^2$ - $2500 \mu\text{C}/\text{cm}^2$
- Ashing : using O_2 plasma
 - Assumed isotropic etching.
 - Etch rate= $10.6\text{nm}/\text{min}$: measured by step height measurement
 - Ashing conditions: $T=300\text{K}$; Pressure= 25mtorr ; $\text{O}_2=30\text{sccm}$;
Forward power= 20W

Process details 3: etching conditions

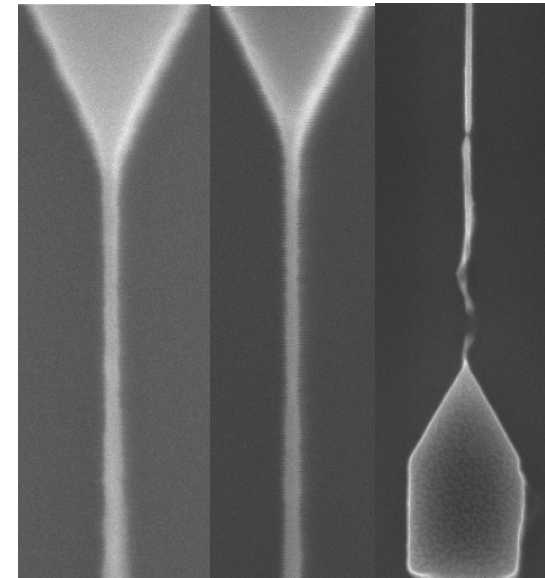
- HBr/Cl₂/O₂ etch chemistry used to etch silicon.
- Selectivity to silicon nitride evaluated using the recipe
- 3-step etch:

	Breakthrough	Main Etch	Overetch
CF ₄ (sccm)	100	0	0
HBr (sccm)	0	150	200
Cl ₂ (sccm)	0	50	0
O ₂ (sccm)	0	0	1
Pressure (mtorr)	13	12	35

Results : Exposure on blank wafer

- Ashed resist feature size $\sim 11\text{nm}$
- Smallest final feature size $\sim 15\text{nm}$: proposed process works
- Oxygen plasma not very isotropic: pressure could have been higher
- Dose inadequate : lot of CD variation and broken lines
- Pattern transfer : some of the gates look discontinuous.

Drawn lines were probably too long to be supported well by the pads at the ends!

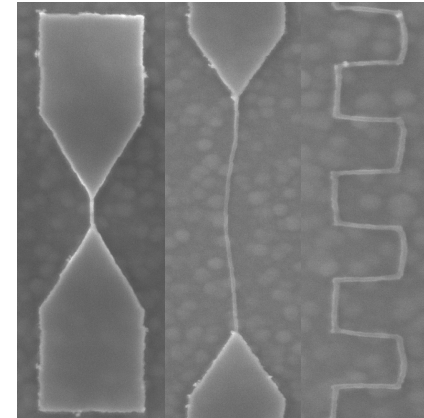


(a) (b) (c)

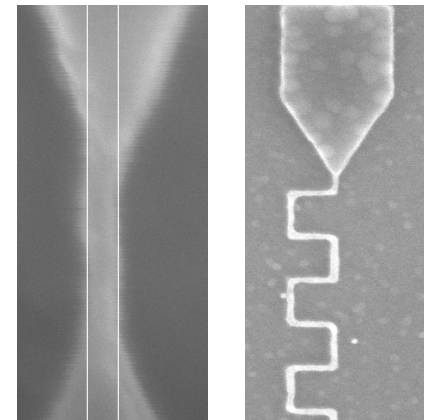
- a. Pre ashing 20nm line
b. Post ashing 20nm line
c. Post etching 20nm line

Results : Exposure on gate stack

- Stack composed of 80Å silicon nitride under 500Å amorphous silicon
- Smallest feature on resist $\sim 10\text{nm}$
- Typical 20 nm feature on resist $\sim 15\text{nm}$
- Final gate widths on silicon $\sim 25\text{nm}$
- No ashing done since wafer was still underexposed!
- Bending observed in $1.5\mu\text{m}$ gates.
- Wiggled gates showed good mechanical stability
- Selectivity to nitride not very high
- *HF etched away thin silicon gates!*



Just developed resist



Transferred silicon features

Failures and their possible causes

- Bent and broken gates :
 - Dose too low (CD variation)
 - Lines too long (broken lines)
 - Bending caused by introducing wet etch followed by rinsing and blow drying on wafer
- Poor pattern transfer from AZPN to silicon:
 - Exposure 1: deep trenches might have tapered the top of the gate and provided no contrast to be viewed under SEM
 - Exposure 2: Narrow silicon gates etched away during HF dip to strip HSQ!

Conclusions

- Sub-20nm resist patterns can be obtained using e-beam lithography followed by resist ashing: SEM numbers are not very reliable at such dimensions.
- Line width/length ratio should typically not be more than about 100.
- Wiggled gates have excellent mechanical stability
- Selectivity of $\text{HBr}/\text{Cl}_2/\text{O}_2$ etch recipe to silicon nitride not very high.
- HF etch can etch thin silicon films!